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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,292	03/12/2004	Kyoung-woo Lee	SAM-0560	8218

7590

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EXAMINER

SARKAR, ASOK K

ART UNIT

PAPER NUMBER

2891

DATE MAILED: 08/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/799,292	LEE ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Asok K. Sarkar	2891	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 July 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-36 is/are pending in the application.
- 4a) Of the above claim(s) 1-15 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 16-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 10, 2006 has been entered.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 16 and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogawa, US 2003/0012117.

Regarding claim 16, Ogawa teaches a dual damascene interconnection structure with a metal – insulator – metal capacitor, the structure comprising:

- a via – level intermetal dielectric 22 and a trench – level intermetal dielectric 41 which are sequentially stacked on a substrate 10;

- a dual damascene interconnection 42/30C formed in the via – level intermetal dielectric and the trench – level intermetal dielectric including a line trench extending through the trench – level intermetal dielectric to the via – level intermetal dielectric; and
- a metal – insulator – metal capacitor MC formed between the via – level intermetal dielectric and the trench – level intermetal dielectric to include a lower electrode 32a, a dielectric layer 34, and an upper electrode 35 with reference to Fig. 1A and corresponding text in paragraphs 37 – 41.

Regarding claim 27, Ogawa teaches a dual damascene interconnection is formed with Cu in paragraph 42.

4. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Kai, US 6,746,914.

Kai teaches all limitations of claim 16 as shown with respect to Fig. 5 in terms of trench, via and the MIM capacitor. Furthermore, the structure has the lower electrode 18, the dielectric layer 20, and the upper electrode 22 are patterned to have the same area with respect to Fig. 5.

5. Claim 22 is rejected under 35 U.S.C. 102(e) as being anticipated by Yoshitomi, US 6,740,974.

Yoshitomi teaches all limitations of claim 16 as shown with respect to Fig. 16 in terms of trench, via and the MIM capacitor. Furthermore, the upper electrode 119 is patterned to have a smaller area than that of each of the lower electrode 116 and the capacitor dielectric layer 117.

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 17 – 20, 23, 28 – 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kai, US 6,746,914 in view of Ogawa, US 2003/0012117.

Regarding claim 17, Kai teaches a via 14 which is included in the via – level

intermetal dielectric 12 to connect the lower electrode 18 and an upper metal interconnection 28 formed on and connected to the upper electrode 22 with reference to Fig. 5.

Kai teaches that the the surface layer 10 is formed on active semiconductor devices to which the present connections of fig. 5 are connected to in column 3, lines 1 – 10, but fails to teach a first lower metal interconnection and a second lower metal interconnection, which are formed between the substrate and the via – level intermetal dielectric and the via is connected to first lower metal interconnection and wherein the dual damascene interconnection is connected to the second lower metal interconnection.

Ogawa teaches a first lower metal interconnection 20a and a second lower metal Interconnection 21b, which are formed between the substrate 10 and the via – level intermetal dielectric 22 and the via 30a is connected to first lower metal interconnection 20a and wherein the dual damascene interconnection is connected to the second lower metal interconnection 21b with reference to Fig. 1a for the benefit of forming a densely arranged memory cells in paragraph 23.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Kai and form a first lower metal interconnection and a second lower metal interconnection, which are formed between the substrate and the via – level intermetal dielectric and the via is connected to first lower metal interconnection and wherein the dual damascene interconnection is connected to the

second lower metal interconnection for the benefit of forming a densely arranged memory cells as taught by Ogawa in paragraph 23.

Regarding claim 18, Ogawa teaches the first lower metal interconnection and the second lower metal interconnection are damascene interconnections buried in an insulating layer formed on the substrate with reference to Fig. 1A.

Regarding claims 19, 20 and 23 Kai teaches the via is filled in a hole - type opening or line – type opening or formed integrally with the lower electrode (see Fig. 5). These are product by process claims.

Note that a “product by process” claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); *In re Marosi et al*, 218 USPQ 289; and particularly *In re Thorpe*, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a “product by process” claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in “product by process” claims or not. Note that applicant has the burden of proof in such cases, as the above case laws make clear.

Regarding claim 28, Ogawa teaches the via and the dual damascene interconnection are formed of different materials in paragraphs 38 and 41.

Regarding claim 29, Kai teaches the limitations as was described earlier in rejecting claim 17.

Regarding claims 30 – 33, Ogawa teaches the limitations with reference to Fig. 5.

10. Claims 14 – 26 and 34 – 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshitomi, US 6,740,974 in view of Ning, US 6,750,115.

Regarding claims 24 and 25, Yoshitomi fails to teach forming an alignment key

in the via – level intermetal dielectric so as to have the step difference to align the metal – insulator – metal capacitor and the key comprising the metal layer for the lower electrode, the dielectric layer, and the metal layer for the upper electrode on the inner walls of the alignment key.

Ning teaches forming an MIM capacitor in which an alignment key 24 is formed in the intermetal dielectric 20 so as to have the step difference to align the metal – insulator – metal capacitor and the key comprising the metal layer for the lower electrode, the dielectric layer, and the metal layer for the upper electrode 42 on the inner walls of the alignment key 24 with reference to Fig. 6 in column 7, lines 18 – 25 for the benefit of assuring correct alignment of various layers with one another in column 2, lines 7 – 12.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Yoshitomi and form an alignment key in the intermetal dielectric so as to have the step difference to align the metal – insulator – metal capacitor and the key comprising the metal layer for the lower electrode, the dielectric layer, and the metal layer for the upper electrode on the inner walls of the alignment key for the benefit of assuring correct alignment of various layers with one another as taught by Ning in column 2, lines 7 – 12.

It would have been obvious to one with ordinary skill in the art at the time of the invention to form the key in the via – level dielectric since the lower electrode of the MIM capacitor of Yoshitomi is also formed in the via – level dielectric.

Regarding claim 26, Yoshitomi in view of Ning fails to teach forming a dummy interconnection in a stepped region of the alignment key.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to form a dummy interconnection in a stepped region of the alignment key since during the forming of the plug in the trench of the trench level or via level dielectric, the step in the key can also be filled with the same material with resorting to an extra processing step to cover it up and filling the plug is usually done after forming the MIM capacitor layers and patterning the layers.

Regarding claims 34 – 36, the limitations of the claims have been described earlier in rejecting claims 22 and 24 – 26.

### ***Conclusion***

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2891

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Asok K. Sarkar  
August 3, 2006

Primary Examiner